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TITLE: Method of verifying a semiconductor integrated circuit apparatus, which can sufficiently evaluate a reliability of a non-destructive fuse module after it is assembled

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TITLE - TI (1):
Method of verifying a semiconductor integrated circuit apparatus, which can sufficiently evaluate a reliability of a non-destructive fuse module after it is assembled

Brief Summary Text - BSTX (3):
The present invention relates to a method of verifying a semiconductor integrated circuit apparatus, which can sufficiently evaluate a reliability of a non-destructive fuse module after it is assembled, and a semiconductor integrated circuit apparatus.

Brief Summary Text - BSTX (6):
A method of using a fuse that can be programmed by carrying out a physical destruction through a laser and the like is typically done in setting a defective address in such a redundancy circuit. In a relieving method of cutting away the fuse through the above-mentioned laser, storing a defective address information, comparing with an input address and replacing with a spare memory line or a spare memory row, the fuse must be cut away before a memory chip is sealed in a package. For this reason, it is impossible to relieve a defect induced after the memory chip is sealed in the package. This results in a trouble that a sufficient improvement of a yield can not be attained.

Brief Summary Text - BSTX (7):
So, a technique is proposed for installing a non-volatile memory such as EEPROM (Electrical Erasable Programmable Read Only Memory) and EPROM (Electrical Programmable Read Only Memory) in a chip of DRAM (Dynamic Random Access Memory) and storing a defective address information as a non-destructive fuse.

Brief Summary Text - BSTX (9):
There is the technique for improving the yield by mounting the fuse in order

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Dono

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(54) METHOD OF VERIFYING A SEMICONDUCTOR INTEGRATED CIRCUIT APPARATUS, WHICH CAN SUFFICIENTLY EVALUATE A RELIABILITY OF A NON-DESTRUCTIVE FUSE MODULE AFTER IT IS ASSEMBLED

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(30) Foreign Application Priority Data

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(51) Int. Cl.[7] G11C 16/06

(52) U.S. Cl. 365/185.22; 365/189.05; 365/189.07

(58) Field of Search 365/185.22, 185.01, 365/189.07, 200, 201, 230.03, 230.08, 189.05

(56) References Cited

U.S. PATENT DOCUMENTS

6,512,101 B2 * 1/2003 Saito et al. 365/200
6,538,921 B2 * 3/2003 Dono et al. 365/185.09

FOREIGN PATENT DOCUMENTS

JP 2001-229690 8/2001
JP 2002-025299 1/2002

OTHER PUBLICATIONS

Shibata, et al., "CMOS Process fli-Flash (Inverse Gate Electrode Flash) Technology for System-on-a Chip", Oct. 2000.

* cited by examiner

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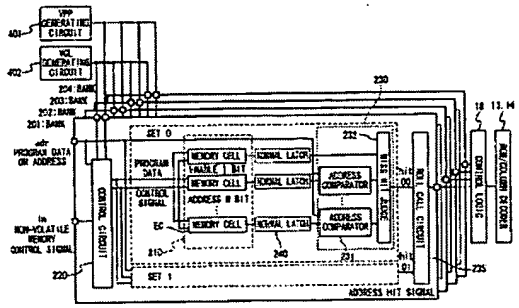
(57) ABSTRACT

A method of verifying a semiconductor integrated circuit apparatus includes (a) providing a semiconductor integrated circuit apparatus including: a first transistor which has a floating gate in which a potential is floated and to which data is written; a second transistor which has a floating gate connected together with the floating gate and reads out the data written to the first transistor; and a control gate unit, which is coupled to the floating gate, controlling an operation of reading out the data of the second transistor; (b) comparing a first data outputted through the second transistor when a first potential is applied to the control gate unit with a second data outputted through the second transistor when a second potential is applied to the control gate unit to generate a comparison result; and (c) verifying the data written to the floating gate based on the comparison result.

22 Claims, 14 Drawing Sheets



Summary of Invention Paragraph - BSTX (8):
[0006] A defective address is found in a wafer test, and programmed in the fuse circuit. After the fuse circuit programming, an input address is transferred to the fuse circuit and compared with the programmed defective addresses. If address matching is detected, decode circuits are controlled by the detected output to replace a defective cell array with a redundant cell array.

Summary of Invention Paragraph - BSTX (9):
[0007] Fuse circuits are used for storing not only the above-described defective addresses, but also many kinds of initial set-up data (i.e., initializing data) that are used for determining memory operation conditions. Such initial set-up data include, for example, trimming data for adjusting internal voltages in corresponding to a process variation among wafers or chips, another trimming data for adjusting programming voltage, control parameters such as sequence loop numbers of program and/or erase sequence, and the like.

Summary of Invention Paragraph - BSTX (10):
[0008] However, once the fuse circuit is programmed, it is impossible to reprogram the fuse circuit. Further, the wafer test for detecting defective addresses by use of a tester and laser-programming process for the fuse circuit are performed as different processes from each other. These processes can not be performed as one continuing step. Considering the above-described viewpoint, it has been provided to use such a system that non-volatile memory cells as similar to that of an EEPROM are used as an initial set-data storing circuit in place of the fuse circuit. By use of such the system, data programming may be performed more easily than the fuse circuit, and data reprogramming may also be performed.

Detail Description Paragraph - DETX (3):
[0021] FIG. 1 shows an EEPROM configuration according to the embodiment of the present invention. Memory cell array 1 is formed of electrically erasable and programmable non-volatile memory cells that are arranged in a matrix manner. Each the memory cell is a stacked-gate type MOS transistor having a floating gate and a control gate stacked thereon. In the memory cell array 1, redundant row cell array 2a and redundant column cell array 2b are disposed for replacing defective cells. An initial set-up data region 3 in the cell array 1 is predefined as a region for programming initial set-up data that are used for determining memory operation conditions.

Detail Description Paragraph - DETX (28):
[0046] The defective address data latch circuit 13, voltage adjustment data latch circuit 15 and chip information data latch circuit 18 are composed as similar to the clock cycle adjustment data latch circuit 22. A select circuit 21 is prepared to transfer the sequentially read out data from the initial set-up data region 3 of the memory cell array 1 to the respective data latch circuits 13, 15, 18 and 22 in the beginning of power-on.

Detail Description Paragraph - DETX (38):
[0056] When the initializing operation is ended, ready/busy(R/B)="H" (ready state) is output, thereby enabling ordinary data read, program and erase operations. In these ordinary operation modes, when an address is input to address register 12, the input address is compared with the defect address stored in the defective address data latch circuit 13 by the address matching detecting circuit 14. When address matching is detected, the detecting circuit 14 outputs replace control signals "Ra" and "Rb", thereby controlling the row decoder 4 and column decoder 7. As a result, a defective cell array including a defect cell is replaced with a redundant cell array. Further, the voltage

NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based upon and claims the benefit of priority from the prior Japanese Application No. 2001-376603, filed on Dec. 10, 2001, the entire content of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a non-volatile semiconductor device.

[0004] 2. Description of Related Art

[0005] A large scale semiconductor memory device is formed to contain redundant circuits for replacing defective cells with them. It's the same to an electrically erasable and programmable non-volatile semiconductor memory device (EEPROM). In a conventional redundant system, a redundant row cell array and a redundant column cell array are disposed in addition to a normal cell array, and a fuse circuit is disposed for storing defective addresses. Such the fuse circuit is typically formed by use of laser-programming type fuses.

[0006] A defective address is found in a wafer test, and programmed in the fuse circuit. After the fuse circuit programming, an input address is transferred to the fuse circuit and compared with the programmed defective addresses. If address matching is detected, decode circuits are controlled by the detected output to replace a defective cell array with a redundant cell array.

[0007] Fuse circuits are used for storing not only the above-described defective addresses, but also many kinds of initial set-up data (i.e., initializing data) that are used for determining memory operation conditions. Such initial set-up data include, for example, trimming data for adjusting internal voltages in corresponding to a process variation among wafers or chips, another trimming data for adjusting programming voltage, control parameters such as sequence loop numbers of program and/or erase sequence, and the like.

[0008] However, once the fuse circuit is programmed, it is impossible to reprogram the fuse circuit. Further, the wafer test for detecting defective addresses by use of a tester and laser-programming process for the fuse circuit are performed as different processes from each other. These processes can not be performed as one continuing step. Considering the above-described viewpoint, it has been provided to use such a system that non-volatile memory cells as similar to that of an EEPROM are used as an initial set-data storing circuit in place of the fuse circuit. By use of such the system, data programming may be performed more easily than the fuse circuit, and data reprogramming may also be performed.

[0009] However, if a cell array for storing defective addresses and the like is disposed at a different place from the normal cell array area, decode circuits and sense amp circuits are necessary for the respective cell arrays. Therefore, the circuit configuration becomes to be complicated, and the chip size becomes large. Additionally, in such a case that check and correct of the programmed data is required, operation control thereof is not easy.

[0010] In order to solve such the problems, the present inventors have already provided such a system that an initial set-up data region is defined in the normal cell array (see, Japanese Patent Application 2001-175290A). The initial set-up data stored in the initial set-up data region in the cell array are automatically read out after when the power supply is switched on by use of the same decoder and sense amp as used in normal data read mode, and then transferred to and held in the respective initial set-up data latch circuits. Hereinafter, the memory operation conditions are defined by the outputs of the initial set-up data latch circuits.

[0011] By use of such the system, the circuit configuration becomes simpler, and the chip size becomes smaller. Check and correct of the initial set-up data can also be performed easily. In this system, the period from power-on time to the initial set-up end becomes a waiting period while normal data read and normal data program are inhibited. Therefore, in such a case that the amount of the initial set-up data is large and/or verify operations are requested, it is necessary to shorten the above-described waiting period if possible.

[0012] Another reason why the waiting period becomes long is in such a fact that the initial set-up data are read out by an internal clock signal generated in the memory chip. While the internal clock is not adjusted by a trimming data that is prepared for canceling process variations, the clock cycle of the internal clock has a large variation. If the clock cycle is shifted to a long-cycle side, the waiting period will become long. Further, the read operation of the initial set-up data is performed as soon as power-on, the power supply voltage is not yet stable. This also leads the waiting period to be long.

SUMMARY OF THE INVENTION

[0013] A non-volatile semiconductor memory device is provided to include a memory cell array having electrically erasable and programmable non-volatile memory cells, a part of the memory cell array being defined as a initial set-up data region for storing a plurality of initial set-up data that define memory operation conditions, data latch circuits for holding the initial set-up data read out from the initial set-up data region, a controller for controlling data program and erase operations for the memory cell array, and a clock generator for generating a clock signal that is used to define an operation timing of the controller, wherein the controller is configured to perform such an initial set-up operation that sequentially reads out the plurality of initial set-up data stored in the initial set-up data region and transfers them to the respective data latch circuits on receipt of power-on or a command input, the initial set-up operation being so performed as to read out a clock cycle adjustment data within the plurality of initial set-up data stored in the initial set-up data region in the beginning, thereby adjusting a clock cycle of the clock signal output from the clock generator by use of the clock cycle adjustment data, and then read out the remaining initial set-up data by use of the adjusted clock signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 shows an EEPROM configuration according to an embodiment of the present invention.